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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,658	11/18/2003	Chung-Peng Hao	10113191	5356

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EXAMINER	
WILSON, CHRISTIAN D	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,658	HAO ET AL.	
	Examiner	Art Unit	
	Christian Wilson	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 18 November 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: search history.

DETAILED ACTION

Claim Objections

1. Claim 21 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 10. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k). For purposes of examination, it will be assumed that claim 21 should depend from claim 11.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 5 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee *et al.* in view of Mandelman *et al.*

Lee *et al.* (US 6,475,916) teaches a damascene gate process comprising providing a semiconductor substrate **10** having a pad layer **14** and an etch stop layer **16**, forming an insulating layer **17** to cover the etch stop layer, forming an opening by partially removing the insulating layer, etch stop layer, and pad layer [Figure 11], forming a protective spacer **25** on the sidewall of the opening where the tops of the protective spacer are lower than the insulating layer

[Figure 13], and forming a gate conducting layer **24** in the opening. Lee *et al.* further discusses forming an LDD region [column 1, lines 25-30], but does not discuss the particular steps to form the LDD regions. Mandelman *et al.* (US 6,674,139) teaches a method of forming LDD regions in a damascene gate structure by removing the protective spacer and insulating layer to expose a portion of the semiconductor substrate and etch stop layer [Figure 7], implanting the exposed substrate to form LDD regions [Figure 8], forming a gate spacer to cover the gate conducting layer [Figure 10], removing the etch stop layer and pad layer to expose the semiconductor substrate [Figure 10], and implanting the substrate to form source/drain regions [Figure 10]. It would have been obvious to one of ordinary skill in the art to use the LDD method of Mandelman *et al.* in the method of Lee *et al.* since this method provides uniform doping of LDD regions.

Regarding claim 2, Lee *et al.* further teaches an oxide layer for the pad layer [column 7, lines 48].

Regarding claim 3, Lee *et al.* further teaches a nitride layer for the etch stop layer [column 7, line 49].

Regarding claim 4, Lee *et al.* further teaches a TEOS layer for the insulating layer [column 7, line 50].

Regarding claim 5, Lee *et al.* further teaches nitride layers for the protective spacers [column 9, line 8].

Regarding claim 9, Lee *et al.* further teaches forming a gate oxide layer **22** on the bottom of the opening.

4. Claims 6, 7, 8, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee *et al.* and Mandelman *et al.* as applied to claim 1 above, and further in view of Dokumaci *et al.*

Regarding claims 6 and 7, Lee *et al.* teaches a gate conducting layer formed of polysilicon, but does not discuss a laminated construction. Dokumaci *et al.* (US 2004/0135212) teaches a laminated conductor layer [0041]. It would have been obvious to one of ordinary skill in the art to use the laminated construction of Dokumaci *et al.* since this provides a gate layer with improved resistance.

Regarding claim 8, Dokumaci *et al.* further teaches a nitride layer for the gate spacer [0044]. It would have been obvious to one of ordinary skill in the art to use the nitride layer of Dokumaci *et al.* since this is a well known material for protecting gate stacks.

Regarding claim 10, Dokumaci *et al.* further teaches using HF to remove insulating layers [0041]. It would have been obvious to one of ordinary skill in the art to use the HF etch of Dokumaci *et al.* to remove the insulating layer of Lee *et al.* since HF is a well known etchant for selective etching of oxide materials.

5. Claims 11 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee *et al.* in view of Mandelman *et al.* and Dokumaci *et al.*

Lee *et al.* teaches a damascene gate process comprising providing a semiconductor substrate **10** having an STI structure **12** with a protective layer [column 5, lines 45-50], sequentially forming a pad layer **14** and an etch stop layer **16** between the STI structures, forming an insulating layer **17** to cover the etch stop layer and STI structures, forming an opening by partially removing the insulating layer, etch stop layer, and pad layer [Figure 11], forming a protective spacer **25** on the sidewall of the opening where the tops of the protective

spacer are lower than the insulating layer [Figure 13], and forming a gate conducting layer **24** in the opening. Lee *et al.* further discusses forming an LDD region [column 1, lines 25-30], but does not discuss the particular steps to form the LDD regions or a conducting layer formed of dissimilar materials. Mandelman *et al.* teaches a method of forming LDD regions in a damascene gate structure by removing the protective spacer and insulating layer to expose a portion of the semiconductor substrate and etch stop layer [Figure 7], implanting the exposed substrate to form LDD regions [Figure 8], forming a gate spacer to cover the gate conducting layer [Figure 10], removing the etch stop layer and pad layer to expose the semiconductor substrate [Figure 10], and implanting the substrate to form source/drain regions [Figure 10]. Dokumaci *et al.* teaches a gate conducting layer formed of dissimilar materials [Figure 7a]. It would have been obvious to one of ordinary skill in the art to use the LDD method of Mandelman *et al.* and the gate conducting layers of Dokumaci *et al.* in the method of Lee *et al.* since this method provides uniform doping of LDD regions and reduced gate conductor line resistance.

Regarding claim 12, Lee *et al.* further teaches oxide layers for the STI structures [column 5, lines 25-35].

Regarding claim 13, Lee *et al.* further teaches a nitride layer for the STI protective layer [column 5, line 48].

Regarding claim 14, Lee *et al.* further teaches a nitride layer for the etch stop layer [column 7, line 49].

Regarding claim 15, Lee *et al.* further teaches a TEOS layer for the insulating layer [column 7, line 50].

Regarding claim 16, Lee *et al.* further teaches nitride layers for the protective spacers [column 9, line 8].

Regarding claim 17, Dokumaci *et al.* further teaches a nitride layer for the gate spacer [0044]. It would have been obvious to one of ordinary skill in the art to use the nitride layer of Dokumaci *et al.* since this is a well known material for protecting gate stacks.

Regarding claims 18 and 19, Lee *et al.* teaches a gate conducting layer formed of polysilicon, but does not discuss a laminated construction. Dokumaci *et al.* teaches a laminated conductor layer [0041]. It would have been obvious to one of ordinary skill in the art to use the laminated construction of Dokumaci *et al.* since this provides a gate layer with improved resistance.

Regarding claim 20, Lee *et al.* further teaches forming a gate oxide layer **22** on the bottom of the opening.

Regarding claim 21, Dokumaci *et al.* further teaches using HF to remove insulating layers [0041]. It would have been obvious to one of ordinary skill in the art to use the HF etch of Dokumaci *et al.* to remove the insulating layer of Lee *et al.* since HF is a well known etchant for selective etching of oxide materials.

Regarding claim 22, Lee *et al.* further teaches an oxide layer for the pad layer [column 7, lines 48].

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chong *et al.* teaches a method of forming a damascene gate structure.

7. A copy of the search history (EAST and STN) is enclosed.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian Wilson whose telephone number is (571) 272-1886. The examiner can normally be reached on weekdays, 7:30 AM to 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christian Wilson, Ph.D.
Primary Examiner
Art Unit 2891

CDW